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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,111	01/17/2002	Kevin E. Brehmer	M-12279 US	1813
36257	7590	04/19/2006	EXAMINER	
PARSONS HSUE & DE RUNTZ LLP			QUIETT, CARRAMAH J	
595 MARKET STREET			ART UNIT	PAPER NUMBER
SUITE 1900			2622	
SAN FRANCISCO, CA 94105				

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/053,111	BREHMER ET AL.
	Examiner	Art Unit
	Carramah J. Quiet	2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 06 February 2006.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 6,8,9,13-23 and 26 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-5,7,10-12,24 and 25 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 17 January 2002 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment(s), filed on 02/06/2006, have been entered and made of record. Claims 1-26 are pending.

### ***Response to Arguments***

2. Applicant's arguments filed 02/06/2006 have been fully considered but they are not persuasive.

With respect to claim 1, this claim includes the final step of:

clamping, by a clamp circuit, at least one signal selected from the detected electronic signals and the sampled signals in response to a detecting of at least one over-saturation condition;  
whereby image inversion is at least partially abated.

For this limitation, the Applicant asserts that neither the passage cited in the previous Office Action nor, as far as can be determined, elsewhere in Fossum describes or suggests the clamp as described above. Please note that the passage, col. 8, lines 9-18 of Fossum, cited in the previous Office Action was a typographical error. However, the Examiner respectfully disagrees. It is determined that the clamp as described above is described and suggested elsewhere in Fossum. In col. 7, lines 39-53, Fossum introduces the second embodiment of his invention. Then, in col. 8, lines 27-28, Fossum states that the CMOS system described in the second embodiment is similar to the block diagram to those previously discussed. Based on that the block diagram Fossum is referring to is figure 6, which is discussed in columns 5-7. Particularly, based on the clamp operation described in Fossum (col. 6, line 38 – col. 7, line 37; col. 8, lines 27-44), he inherently teaches the final step of clamping (see above) as recited by the Applicant.

With respect to claim 2, the Applicant believes that this claim is allowable because Fossum does not teach the limitation, "...the photo detector comprises a photo diode." However, the Examiner respectfully disagrees. As stated earlier, in col. 8, lines 27-28, Fossum states that the CMOS system described in the second embodiment is similar to the block diagram to those previously discussed. Based on that, in col. 5, lines 28-40 of Fossum, the photo detector inherently comprises a photodiode because they are on the same substrate.

With respect to claim 5, the Applicant is concerned with the step of:

clamping, with a clamp circuit, signals selected from the image signals and the sampled signals during a reset phase of the correlated double sampler.

The Applicant asserts that Fossum does not provide a discussion of a phase reset in the passage cited in the previous Office Action. Please note that the passage, col. 7, lines 44-53 of Fossum, cited in the previous Office Action was a typographical error. Fossum's invention provides a method for clamping, with a clamp circuit, signals selected from the image signals (col. 6, line 38 – col. 7, line 37) and the sampled signals during a reset phase of the correlated double sampler (col. 8, lines 27-44). Please note that there is a reset phase because Fossum teaches a phase for resetting the output branch, which stores, samples, and holds reset signals (col. 8, lines 27-44). Additionally by reducing column fixed pattern noise (FPN), the sampling operation is completed. Also, please read the entire sampling operation in col. 5, line 65 – col. 7, line 38.

With respect to claim 10, please note that the passage, col. 7, lines 44-53 of Fossum, cited in the previous Office Action was a typographical error. Fossum teaches a clamp circuit operation in col. 6, line 38 – col. 7, line 37 and in col. 8, lines 27-44.

With respect to claim 24, the Applicant asserts that the cited passage from the previous Office Action nor elsewhere does Tsang teach or suggest:

- a. a first sample of a first signal during a first interval after reset of a photo detector;
- b. detecting that the first signal is slewing excessively rapidly during the first interval;
- c. limiting the value of the first sample;
- d. whereby the image sensor produces an output of improved accuracy.

In the previous Office Action, the Examiner cited col. 7, lines 28-67 to show that Tsang teaches this limitation as well as the “second sample” limitation. The upper part of that passage, describes a first sample (first readout mode) of a first signal during a first interval after reset of a photo detector. Particularly, please read col. 7, lines 28-42. Secondly, col. 10, lines 5-38 of Tsang were used to teach detecting that the first signal is slewing excessively rapidly during the first interval. The limitation “detecting that the first signal is slewing excessively rapidly” is taught in col. 10, lines 5-17. Tsang teaches how the high electron voltage conversion gain decreased, during the integration period, thereby reducing leakage current and area (col. 9, line 66 – col. 10, line 10). Then, in col. 10, lines 12-24, the signal is rapidly reset and a higher VRST level is used to improve the dynamic range of the cell. Tsang did not choose to use the words “slewing” and “excessively” to describe the operation. However, he did choose to use words and phrases which have similar representations. Further in the same passage (col. 10, lines 12-24), Tsang limits limiting the value of the first sample by clamping the voltage. This produces antiblooming, which improves the accuracy of displaying the image (col. 10, lines 18-24). Tsang provides an overall improvement in col. 10, lines 31-35.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-3, 5, 7, and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by Fossum et al. (#5,841,126).

As for **claim 1**, Fossum discloses a method for image sensing (second embodiment) comprising the acts of:

producing, from a photo detector, a plurality of detected electronic signals responsive to an optical image (col. 7, lines 44-64).

amplifying, with a column buffer amplifier, signals selected from the detected electronic signals to produce a plurality of amplified signals (col. 7, lines 44-53);

sampling, with a correlated double sampler, signals selected from the amplified signals to produce a plurality of sampled signals (col. 8, lines 27-38); and

clamping, by a clamp circuit, at least one signal selected from the detected electronic signals and the sampled signals in response to a detecting of at least one over-saturation condition; whereby image inversion is at least partially abated (col. 6, line 38 – col. 7, line 37; col. 8, lines 27-44).

For **claim 2**, Fossum discloses the method wherein the photo detector comprises a photo diode (inherently, col. 5, lines 28-40; col. 8, lines 27-28).

For **claim 3**, Fossum discloses the method wherein the photo detector comprises a photo gate (col. 7, lines 44-64).

As for **claim 5**, Fossum discloses a method for enhancing a video image comprising the acts of:

sampling a plurality of image signals with a correlated double sampler (CDS) to produce a plurality of sampled signals (col. 8, lines 27-38);

clamping, with a clamp circuit, signals selected from the image signals (col. 6, line 38 – col. 7, line 37) and the sampled signals during a reset phase of the correlated double sampler (col. 8, lines 27-44). In col. 8, lines 27-28, Fossum states that the CMOS system described in the second embodiment is similar to the block diagram to those previously discussed. Please note that there is a reset phase because Fossum teaches a reset output branch, which stores, samples, and holds reset signals. Additionally by reducing column fixed pattern noise (FPN), the sampling operation is completed. Also, please read the entire sampling operation in col. 5, line 65 – col. 7, line 38.

For **claim 7**, Fossum discloses the method wherein the clamp circuit operates in conjunction with a column buffer amplifier comprising a source follower (col. 8, lines 27-38).

As for **claim 10**, Fossum discloses a circuit (fig. 8) comprising: an image sensor array (pixel array) comprising:

a clamp circuit (col. 6, line 38 – col. 7, line 37; col. 8, lines 27-44);

column buffer amplifier (col. 7, lines 44-64); and

a correlated double sampling circuit (col. 8, lines 27-38).

5. **Claims 24-25** are rejected under 35 U.S.C. 102(b) as being anticipated by Tsang et al. (#5,900,623).

For **claim 24**, Tsang teaches that in an image sensor that correlates a first sample (first readout mode) of a first signal during a first interval after reset of a photo detector and a second sample (second readout mode) of the first signal during a later interval to produce a luminance signal (photo current,  $I_d$  – col. 7, lines 28-67), a method for abating (reducing) an error (blooming) in the luminance signal due to excessively rapid slewing of the first signal during the first interval wherein the improvement (col. 9, line 66 – col. 10, line 24; col. 13, lines 43-54) comprises:

detecting that the first signal is slewing excessively rapidly during the first interval (col. 10, lines 5-38); and

limiting the value of the first sample (col. 10, lines 18-24);  
whereby the image sensor produces an output of improved accuracy (col. 10, lines 31-35).

For **claim 25**, Tsang teaches the method wherein: the error (blooming) is an image inversion due to over-saturation (col. 10, lines 11-24).

#### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (#5,841,126) in view of Koyama et al. (#5,786,713).

For **claim 4**, Fossum teaches the method with a clamp circuit (col. 7, lines 44-53).

However, Fossum does not expressly teach the method wherein the clamp circuit is implemented in a technology selected from a list consisting of N-well CMOS process technology and of P-well CMOS process technology. In a similar field of endeavor, Koyama teaches a method wherein the clamp circuit is implemented in a technology selected from a list consisting of N-well CMOS process technology and of P-well CMOS process technology (fig. 37; col. 20, lines 41-47). In light of the teaching of Koyama, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Fossum's clamp circuit in a technology selected from a list consisting of N-well CMOS process technology and of P-well CMOS process technology in order to control the integration the imaging device (Koyama, col. 20, lines 41-62).

8. **Claims 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (#5,841,126) in view of Yano (#6,900,832).

For **claim 11**, Fossum discloses the circuit wherein the imaging device has 3 modes with different integration periods (col. 7, lines 44-64). However, Fossum does not expressly disclose the circuit wherein the image sensor array captures still images. In a similar field of endeavor, Yano discloses the circuit wherein the image sensor array captures still images (fig. 4, col. 5, lines 50-51). In light of the teaching of Yano, it would have been obvious to one of ordinary skill

in the art at the time the invention was made to provide the imaging device of Fossum with an image sensor array that captures still images in order to improve the quality of imaging for the different modes (Yano, col. 2, lines 16-50).

For **claim 12**, Fossum discloses the circuit wherein the imaging device has 3 modes with different integration periods (col. 7, lines 44-64). However, Fossum does not expressly disclose the circuit wherein the image sensor array captures moving video images. In a similar field of endeavor, Yano discloses the circuit wherein the image sensor array captures moving video images (Yano, col. 6, lines 25-26). In light of the teaching of Yano, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the imaging device of Fossum with an image sensor array that captures moving video images in order to improve the quality of imaging for the different modes (Yano, col. 2, lines 16-50).

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571) 272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CJQ  
April 15, 2006



NGOC-YEN VU  
SUPERVISORY PATENT EXAMINER